ORIGINALLY SUBMITTED INFORMAL DRAWINGS

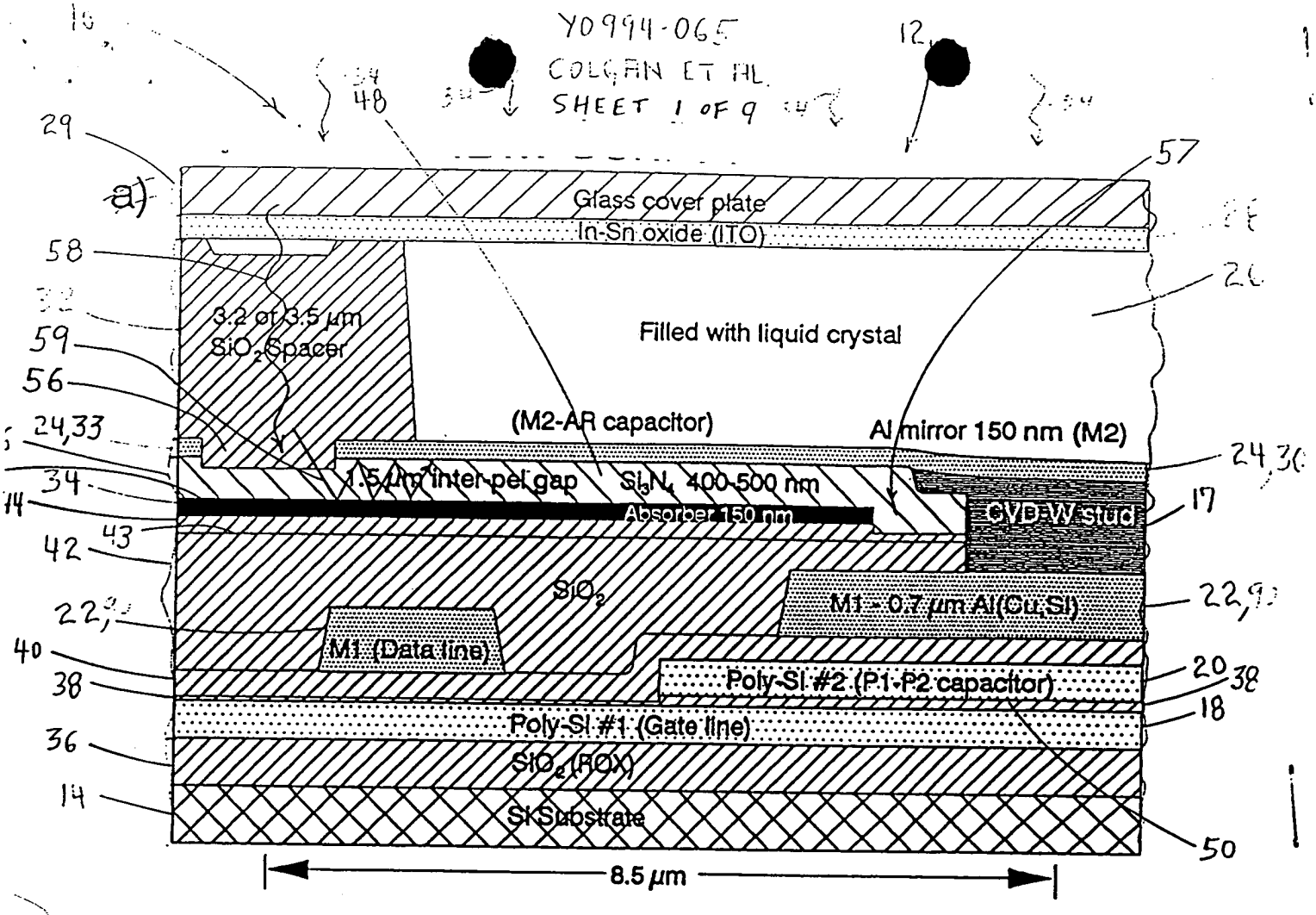


FIG 1

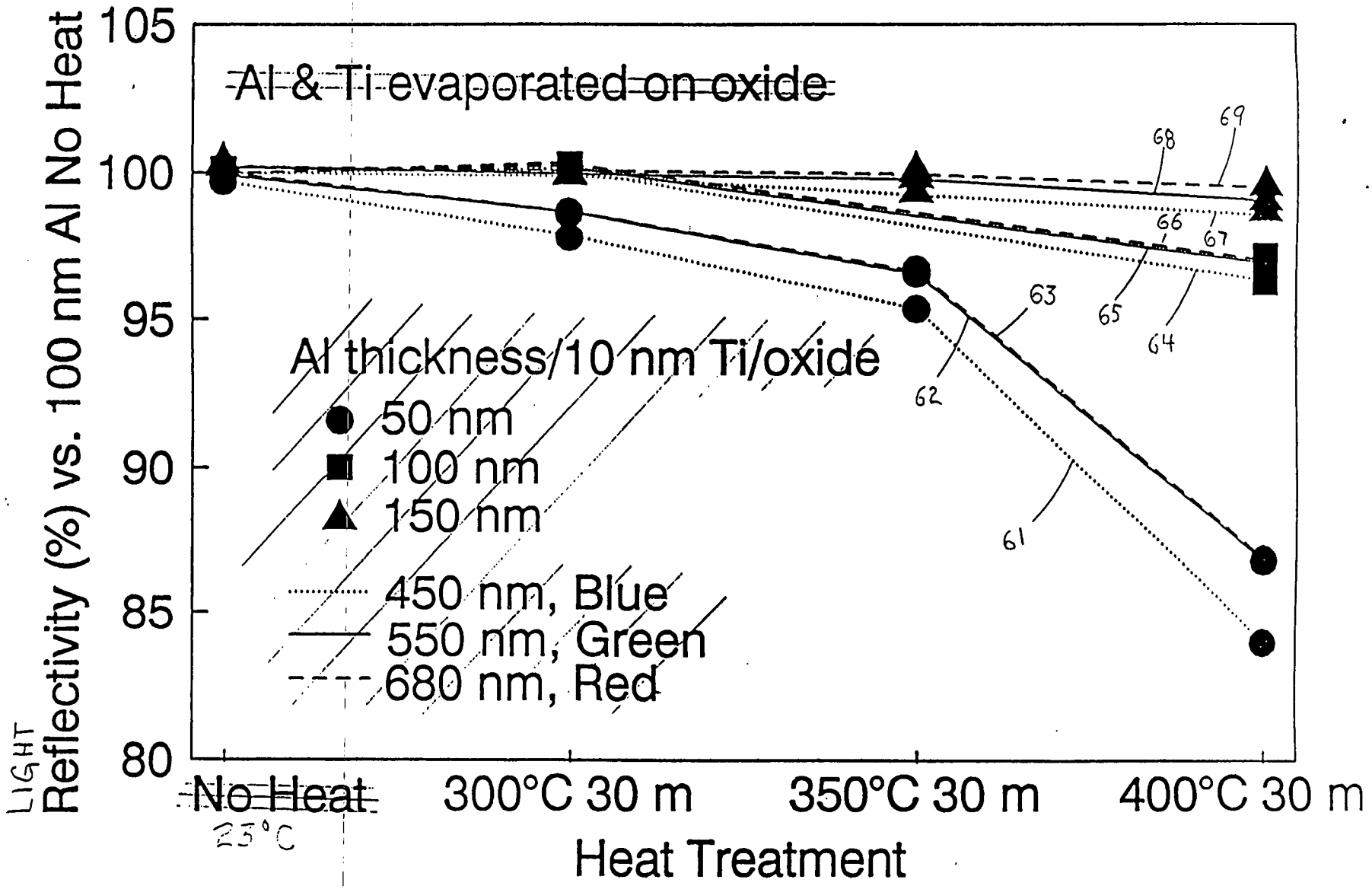


Fig. 2

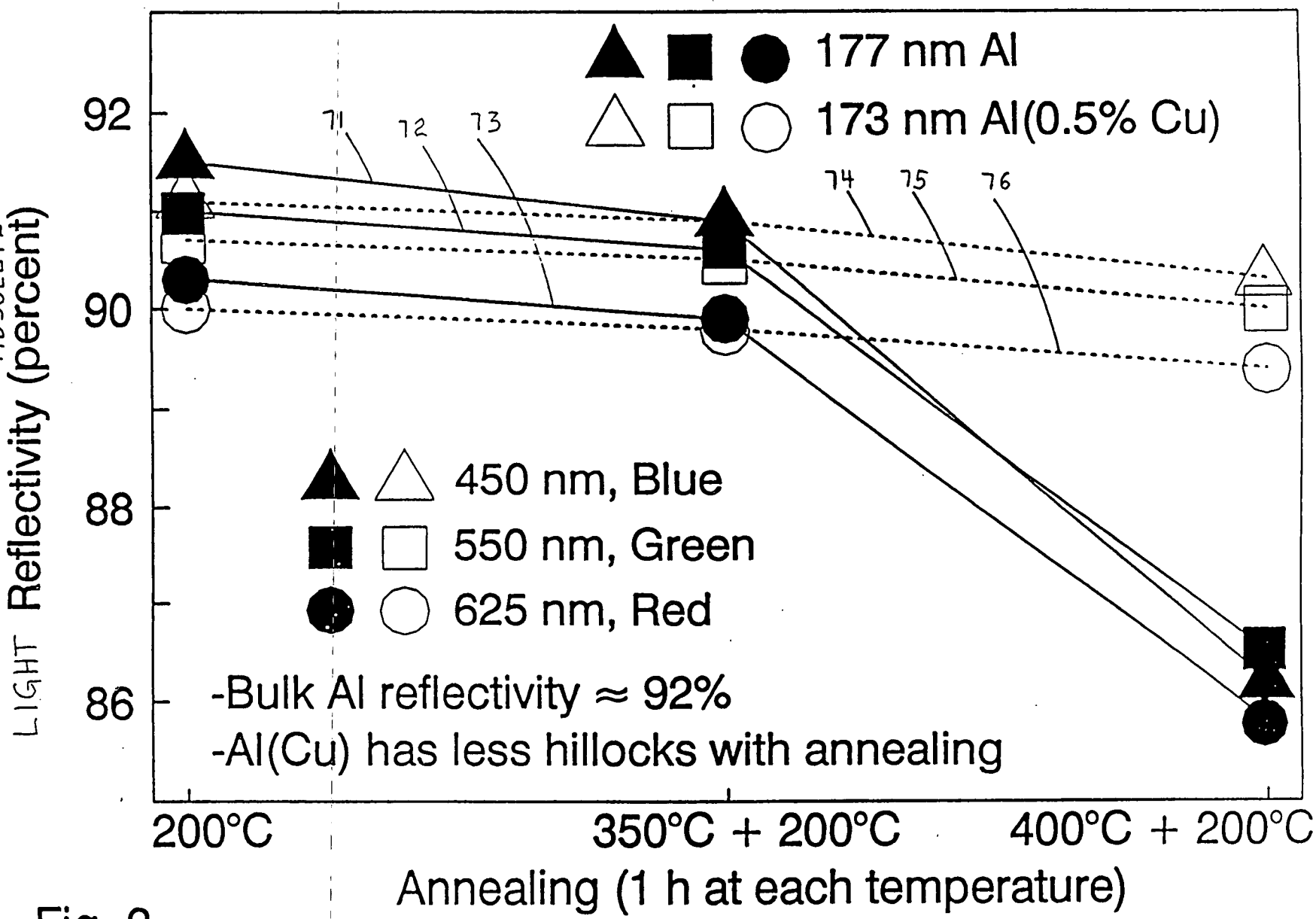


Fig. 3

ARC3

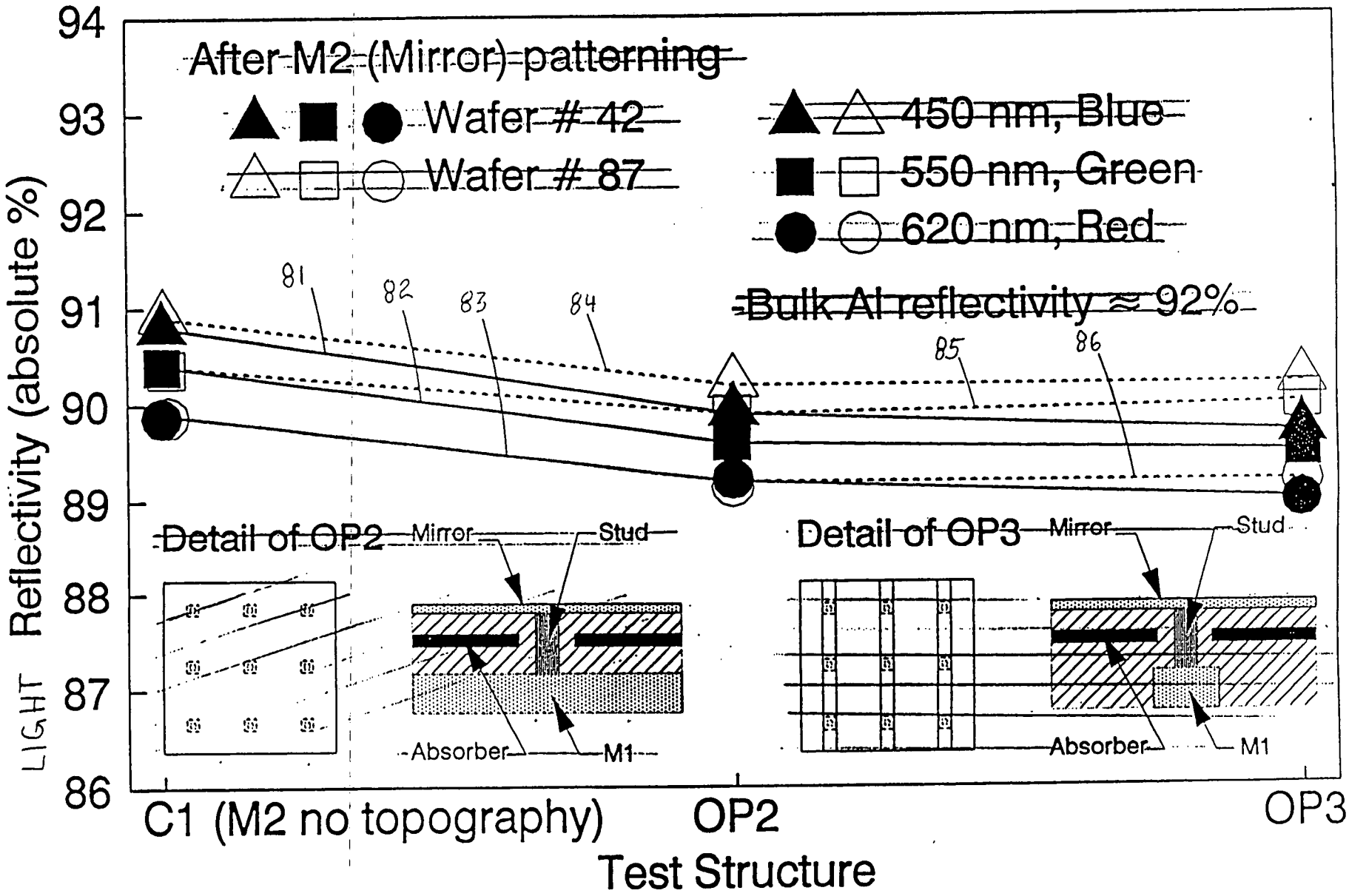


Fig. 4

ARC4

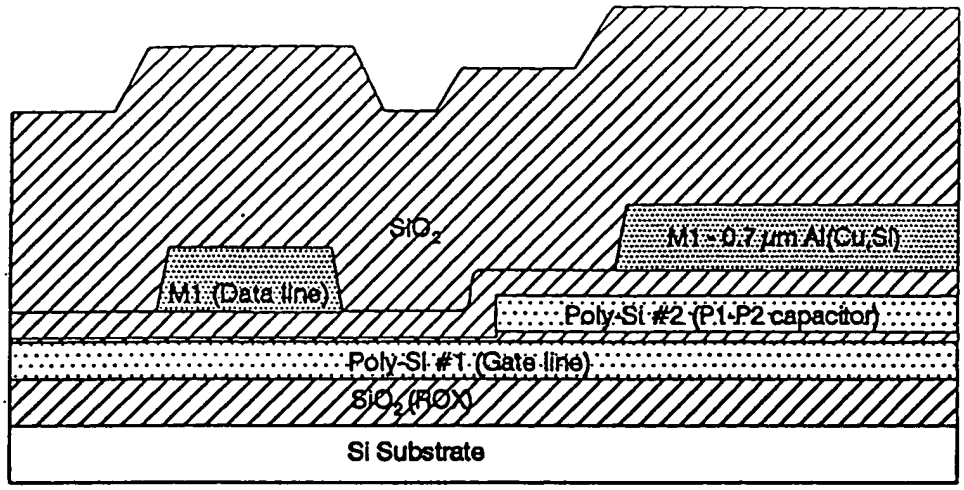


FIG 5

a) Liftoff 0.7 μm Al(Cu,Si) M1.
Deposit thick oxide.

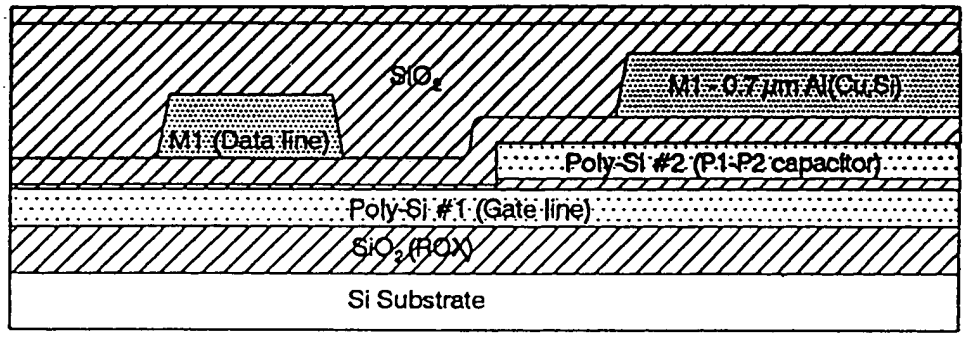


FIG 6

b) CMP oxide leaving 500 nm on highest M1 point.
Deposit 200 nm oxide.

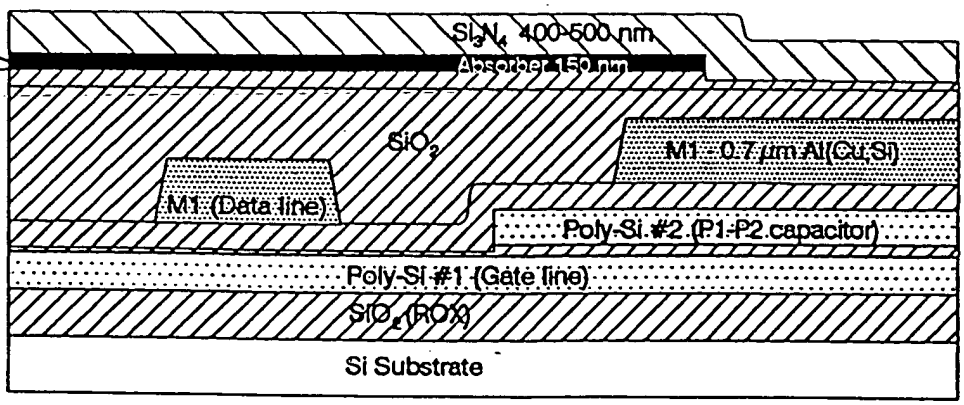
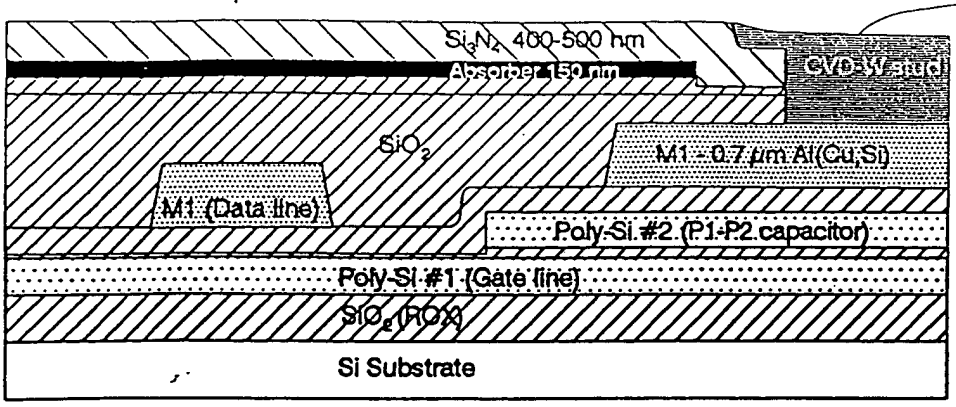


FIG 7

c) Deposit 10 nm Ti/ 100 nm Al/ 50 nm TiN, pattern with AR mask.
Deposit 400-500 nm nitride.

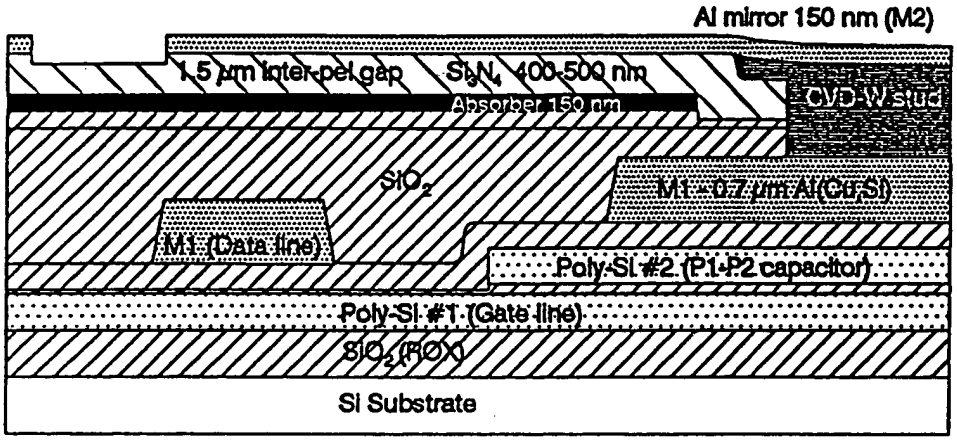
~~Fig. 5(a-c)~~

96



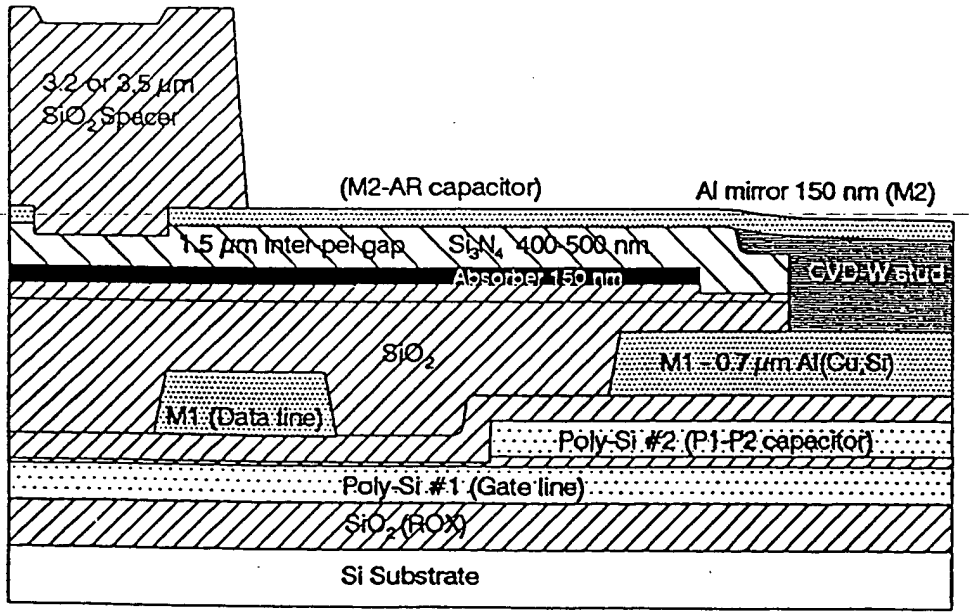
d) Pattern with V1 mask. Deposit liner & CVD-W. W Chem-mech polish.

FIG 8



e) Deposit 10 nm Ti/ 150 nm Al, pattern with M2 mask.

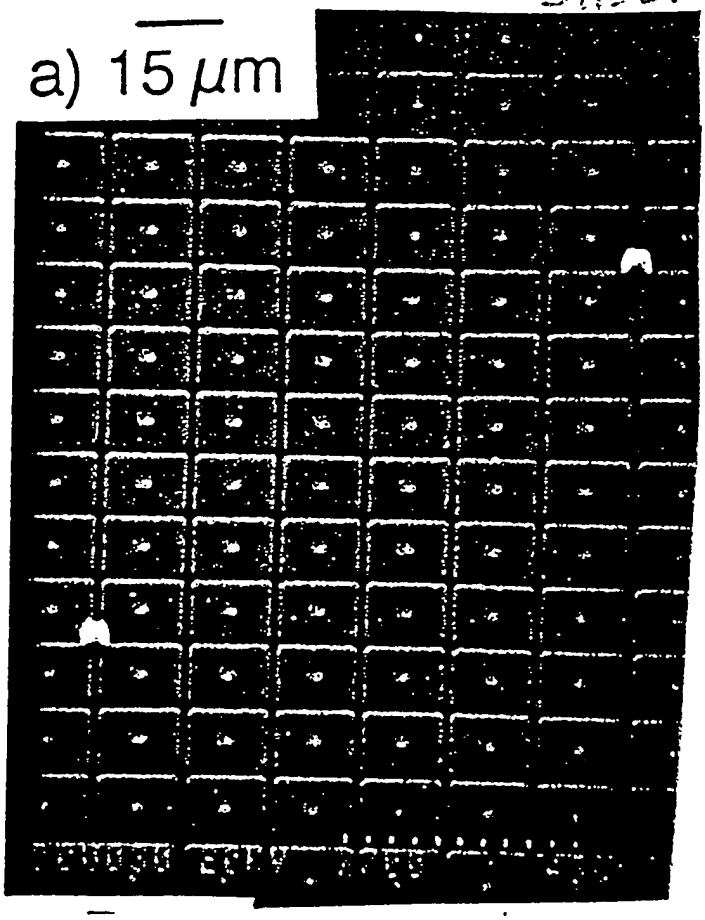
FIG 9



f) Deposit 2.2 or 3 μm oxide, pattern with SP mask. Open up M1 pads with TV mask.

~~Fig. 5(d-f)~~ FIG 10

 ARC5B



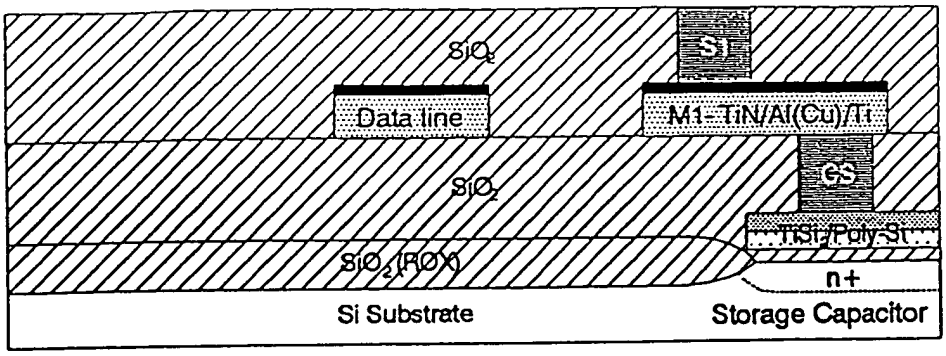


FIG 12

a) Use standard CMOS 4 process to S1.

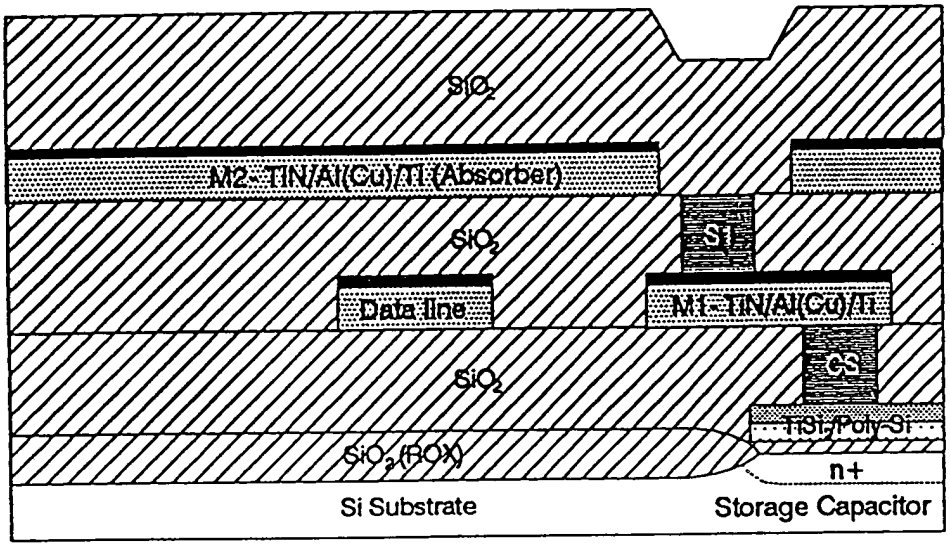


FIG 13

b) Pattern POR M2 as Absorber layer. POR oxide deposition.

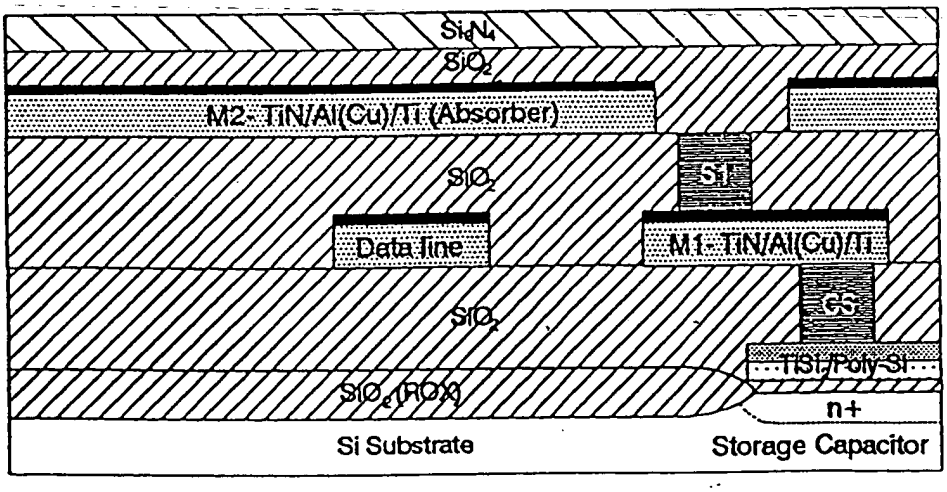


FIG 14

c) CMP-oxide leaving 500 nm on highest M2 point. Deposit 300 nm nitride.

Fig. 8(a-c)

ARC8A

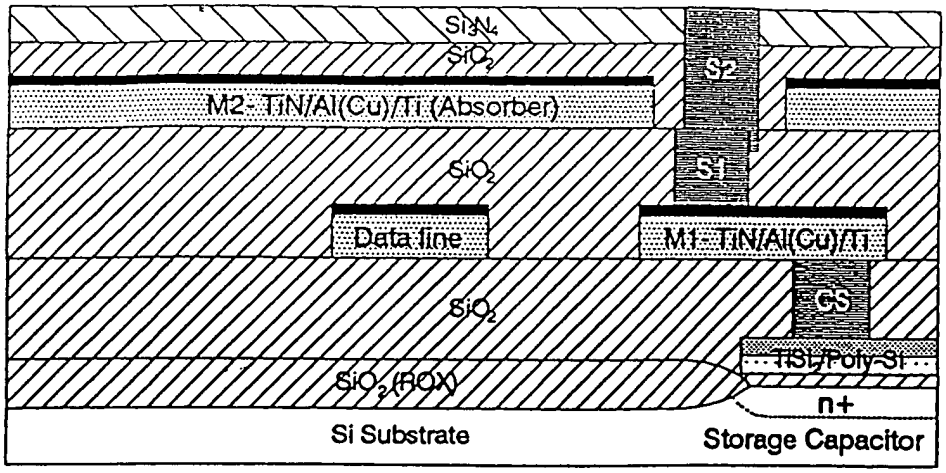


FIG 15

d) Pattern with S2 mask. Deposit liner & CVD-W. W Chem-mech polish. Stacked S1&S2 to connect M1 & M3.

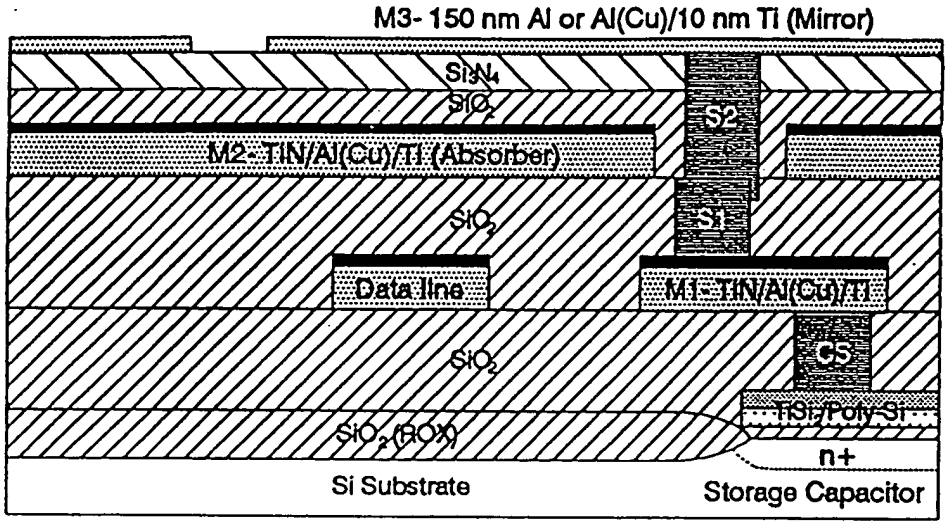


FIG 16

e) Deposit 10 nm Ti/ 150 nm Al, pattern with M3 mask.

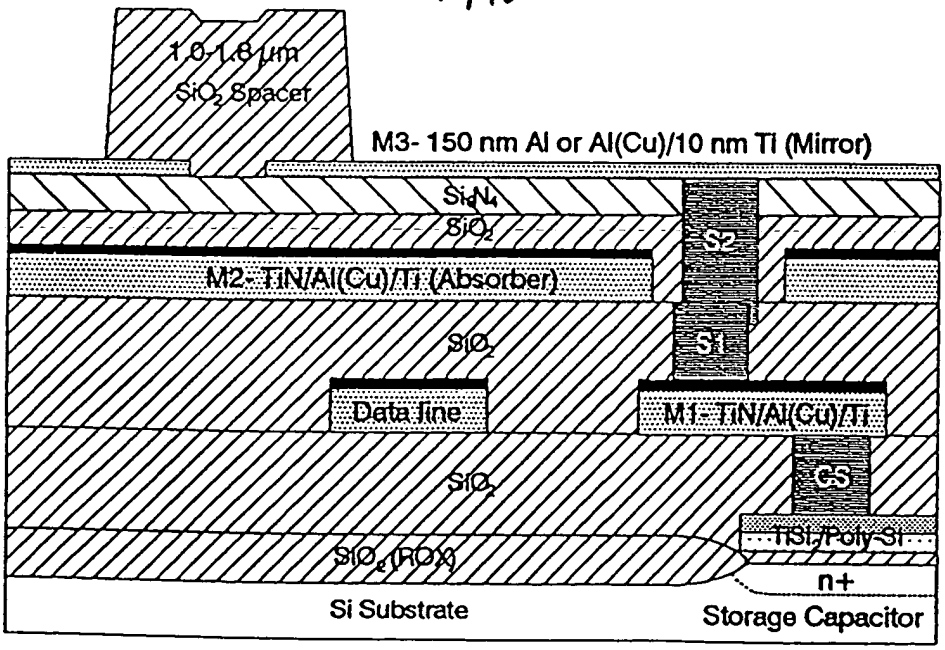


Fig. 8(d-f) FIG 17

f) Deposit 1.0 or 1.8 μm oxide, pattern with SP mask. Open up M2 pads with TV mask.